**VERILOG CODE**

**module** aclock (**input** reset,

**input** clk,

**input** [**1**:**0**] H\_in1,

**input** [**3**:**0**] H\_in0,

**input** [**3**:**0**] M\_in1,

**input** [**3**:**0**] M\_in0,

**input** LD\_time,

**input** LD\_alarm,

**input** STOP\_al,

**input** **AL\_ON**,

**output** **reg** Alarm,

**output** [**1**:**0**]H\_out1,

**output** [**3**:**0**]H\_out0,

**output** [**3**:**0**]M\_out1,

**output** [**3**:**0**]M\_out0,

**output** [**3**:**0**]S\_out1,

**output** [**3**:**0**]S\_out0 );

**reg** clk\_1s;

**reg** [**3**:**0**] tmp\_1s;

**reg** [**5**:**0**] tmp\_hour, tmp\_minute, tmp\_second;

**reg** [**1**:**0**] c\_hour1,a\_hour1;

**reg** [**3**:**0**] c\_hour0,a\_hour0;

**reg** [**3**:**0**] c\_min1,a\_min1;

**reg** [**3**:**0**] c\_min0,a\_min0;

**reg** [**3**:**0**] c\_sec1,a\_sec1;

**reg** [**3**:**0**] c\_sec0,a\_sec0;

**function** [**3**:**0**] mod\_10;

**input** [**5**:**0**] number;

**begin**

mod\_10 = (number >=**50**) ? **5** : ((number >= **40**)? **4** :((number >= **30**)? **3** :((number >= **20**)? **2** :((number >= **10**)? **1** :**0**))));

**end**

**endfunction**

**always** @(**posedge** clk\_1s **or** **posedge** reset )

**begin**

**if**(reset) **begin**

a\_hour1 <= **2'b00**;

a\_hour0 <= **4'b0000**;

a\_min1 <= **4'b0000**;

a\_min0 <= **4'b0000**;

a\_sec1 <= **4'b0000**;

a\_sec0 <= **4'b0000**;

tmp\_hour <= H\_in1\***10** + H\_in0;

tmp\_minute <= M\_in1\***10** + M\_in0;

tmp\_second <= **0**;

**end**

**else** **begin**

**if**(LD\_alarm) **begin**

a\_hour1 <= H\_in1;

a\_hour0 <= H\_in0;

a\_min1 <= M\_in1;

a\_min0 <= M\_in0;

a\_sec1 <= **4'b0000**;

a\_sec0 <= **4'b0000**;

**end**

**if**(LD\_time) **begin**

tmp\_hour <= H\_in1\***10** + H\_in0;

tmp\_minute <= M\_in1\***10** + M\_in0;

tmp\_second <= **0**;

**end**

**else** **begin**

tmp\_second <= tmp\_second + **1**;

**if**(tmp\_second >=**59**) **begin**

tmp\_minute <= tmp\_minute + **1**;

tmp\_second <= **0**;

**if**(tmp\_minute >=**59**) **begin**

tmp\_minute <= **0**;

tmp\_hour <= tmp\_hour + **1**;

**if**(tmp\_hour >= **24**) **begin**

tmp\_hour <= **0**;

**end**

**end**

**end**

**end**

**end**

**end**

**always** @(**posedge** clk **or** **posedge** reset)

**begin**

**if**(reset)

**begin**

tmp\_1s <= **0**;

clk\_1s <= **0**;

**end**

**else** **begin**

tmp\_1s <= tmp\_1s + **1**;

**if**(tmp\_1s <= **5**)

clk\_1s <= **0**;

**else** **if** (tmp\_1s >= **10**) **begin**

clk\_1s <= **1**;

tmp\_1s <= **1**;

**end**

**else**

clk\_1s <= **1**;

**end**

**end**

**always** @(\*) **begin**

**if**(tmp\_hour>=**20**) **begin**

c\_hour1 = **2**;

**end**

**else** **begin**

**if**(tmp\_hour >=**10**)

c\_hour1 = **1**;

**else**

c\_hour1 = **0**;

**end**

c\_hour0 = tmp\_hour - c\_hour1\***10**;

c\_min1 = mod\_10(tmp\_minute);

c\_min0 = tmp\_minute - c\_min1\***10**;

c\_sec1 = mod\_10(tmp\_second);

c\_sec0 = tmp\_second - c\_sec1\***10**;

**end**

**assign** H\_out1 = c\_hour1;

**assign** H\_out0 = c\_hour0;

**assign** M\_out1 = c\_min1;

**assign** M\_out0 = c\_min0;

**assign** S\_out1 = c\_sec1;

**assign** S\_out0 = c\_sec0;

**always** @(**posedge** clk\_1s **or** **posedge** reset) **begin**

**if**(reset)

Alarm <=**0**;

**else** **begin**

**if**({a\_hour1,a\_hour0,a\_min1,a\_min0,a\_sec1,a\_sec0}=={c\_hour1,c\_hour0,c\_min1,c\_min0,c\_sec1,c\_sec0})

**begin**

**if**(**AL\_ON**) Alarm <= **1**;

**end**

**if**(STOP\_al) Alarm <=**0**;

**end**

**endmodule**

**Test bench for alarm clock:**

**module** test;

**reg** reset;

**reg** clk;

**reg** [**1**:**0**] H\_in1;

**reg** [**3**:**0**] H\_in0;

**reg** [**3**:**0**] M\_in1;

**reg** [**3**:**0**] M\_in0;

**reg** LD\_time;

**reg** LD\_alarm;

**reg** STOP\_al;

**reg** **AL\_ON**;

**wire** Alarm;

**wire** [**1**:**0**] H\_out1;

**wire** [**3**:**0**] H\_out0;

**wire** [**3**:**0**] M\_out1;

**wire** [**3**:**0**] M\_out0;

**initial** **begin**

reset = **1**;

H\_in1 = **1**;

H\_in0 = **0**;

M\_in1 = **1**;

M\_in0 = **4**;

LD\_time = **0**;

LD\_alarm = **0**;

STOP\_al = **0**;

**AL\_ON** = **0**;

#**1000**;

reset = **0**;

H\_in1 = **1**;

H\_in0 = **0**;

M\_in1 = **2**;

M\_in0 = **0**;

LD\_time = **0**;

LD\_alarm = **1**;

STOP\_al = **0**;

**AL\_ON** = **1**;

#**1000**;

reset = **0**;

H\_in1 = **1**;

H\_in0 = **0**;

M\_in1 = **2**;

M\_in0 = **0**;

LD\_time = **0**;

LD\_alarm = **0**;

STOP\_al = **0**;

**AL\_ON** = **1**;

**wait**(Alarm);

#**1000**

STOP\_al = **1**;

#**1000**

STOP\_al = **0**;

H\_in1 = **0**;

H\_in0 = **4**;

M\_in1 = **4**;

M\_in0 = **5**;

LD\_time = **1**;

LD\_alarm = **0**;

#**1000**

STOP\_al = **0**;

H\_in1 = **0**;

H\_in0 = **4**;

M\_in1 = **5**;

M\_in0 = **5**;

LD\_alarm = **1**;

LD\_time = **0**;

**wait**(Alarm);

#**1000**

STOP\_al = **1**;

**end**

**endmodule**